What is claimed is:

1. An automatic baud rate detection circuit comprising:

a signal detector which detects first predetermined signals at an input stage of a transceiver and responsive thereto, outputs second predetermined signals;

a reference signal oscillator generator; and

a frequency discriminator which receives a reference signal from the reference signal oscillator generator, and signals from the input stage of the transceiver, and outputs a baud rate signal in response to the second predetermined signals from the signal detector.

2. The circuit according to claim 1, wherein the input stage of the transceiver comprises:

a photodetector which detects optical communications signals and outputs electrical signals'

a linear amplifier coupled to receive the electrical signals from the photodetector at an input and produce output signals at an output thereof; and

a limiting amplifier which receives signals from the linear amplifier output at an input and produces output signals at an output thereof;

wherein the signal detector receives the first predetermined signals from the output of the linear amplifier, and wherein the frequency discriminator receives signals from the output of the limiting amplifier.

3. The circuit according to claim 2, further comprising a decoder which decodes the baud rate signal from the frequency discriminator and produces a decoded output signal.

4. The circuit according to claim 3, wherein:

the linear amplifier comprises a selectable filter; and

the decoded output signal from the decoder is provided to the selectable filter to select a filter configuration appropriate for an associated baud rate.

5. A transceiver arrangement comprising:

a transceiver;

a multiplexer which receives data at a first input and a predetermined digital pattern signal at a second input, and which output either the data or the digital pattern signal at an output depending on a negotiate control signal input signal;

a serializer which receives the output from the multiplexer and provides a serialized output to the transceiver; and

a state machine which outputs a first control signal to the transceiver, and outputs the negotiate control signal to the multiplexer to select the digital pattern signal, responsive to receiving a second control signal from the transceiver.

6. The transceiver arrangement according to claim 5, wherein the state machine comprises:

logic means for receiving the second control signal from the transceiver, and outputting the negotiate control signal to the multiplexer; and

pulse generator means for outputting the first control signal to the transceiver responsive to an enable signal from the logic means, and outputting pulse signals to the logic means.

7. The transceiver arrangement according to claim 5, wherein the logic means comprises:

a first set/reset latch which receives the second control signal from the transceiver at a set input, and outputs the enable signal to the pulse generator means;

a second set/reset latch which receives the enable signal from the first set/reset latch at a set input, and outputs the negotiate control signal;

a D-latch which receives the second control signal from the transceiver at a D input, and outputs a sample in response to a first pulse signal from the pulse generator means at a clock input;

an inverter which inverts the sample from the D-latch; and

an AND gate which receives the inverted sample from the inverter at a first input, a second pulse signal from the pulse generator means at a second input, and outputs the logical AND of the first and second inputs to a reset input of the first set/reset latch and the second set/reset latch.

8. The transceiver arrangement according to claim 5, wherein:

the pulse generator means outputs the first control signal for a time interval greater than the minimum pulse width for the first control signal on the transceiver;

the pulse generator means outputs the first pulse a time interval after the end of the second control signal which is greater than twice a delay on a transmission medium to which the transceiver is coupled, plus response times for the first control signal and the second control signal; and

the pulse generator means outputs the second pulse a time interval after the end of the first pulse which is greater than a lock-on time of a frequency discriminator in the transceiver.

9. A method of automatic baud rate negotiation comprising utilizing the automatic baud rate detection circuit according to claim 1.

10. A transceiver arrangement having a transceiver comprising the automatic baud rate detection circuit according to claim 1, the transceiver arrangement further comprising:

a multiplexer which receives data at a first input and a predetermined digital pattern signal at a second input, and which output either the data or the digital pattern signal at an output depending on a negotiate control signal input signal;

a serializer which receives the output from the multiplexer and provides a serialized output to the transceiver; and

a state machine which outputs a first control signal to the transceiver, and outputs the negotiate control signal to the multiplexer to select the digital pattern signal, responsive to receiving a second control signal from the transceiver.